ABSTRACT OF THE DISCLOSURE

A phase locked loop type frequency synthesizer utilizing a reference signal source includes a voltage controlled oscillator (VCO), a phase comparator, a programmable pre-scaler and a modulator. The programmable pre-scaler divides the output of the VCO according to a sequence of divide ratios to produce a divided signal having a frequency approximating the reference signal frequency. The phase comparator compares the phases of the divided signal and the reference signal and, in response to a difference, adapts the VCO to reduce the detected difference. The modulator provides a next value in the sequence of divide ratios by accumulating an error between a present value and an average value in the sequence of divide ratios, accumulating the accumulated error values, and determining the next value in the sequence of divide ratios such that the multiply-accumulated error values are maintained within finite bounds.